Attorney Docket No.: P-2448-US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	AVNI, Dror et al.	Examiner:	Ho, Hoai V.
Serial No.:	09/730,586	Group Art Unit:	2818
Filed:	December 7, 2000		
Title:	PROGRAMMING AND ERASING METHODS FOR AN NROM ARRAY		

RESPONSE

Mail Stop Non-Fee Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Amendment is filed in response to the Office Action dated July 31, 2003 issued by the United States Patent and Trademark Office in connection with the above-identified Application. A response to the July 31, 2003 Office Action was due October 31, 2003. Applicants are concurrently filing a Petition for a Two-Month Extension of Time, including the required fee. Therefore, this response is due December 31, 2003. Accordingly, this Amendment is being timely filed.

Kindly consider the following:

Arguments begin on page 2 of this paper.

ARGUMENT

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1-14 are pending in the application.

Claims 1-14 have been rejected.

CLAIM REJECTIONS

35 U.S.C. § 112 Rejections

In the Office Action, the Examiner rejected claim 1 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement, arguing that the claims contains subject matter "which was not described in the specification in such a way to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention." Applicants respectfully disagree with the Examiner and traverse this rejection in view of the remarks that follow.

Specifically, Applicants respectfully assert that the specification does contain a sufficient written description of the subject matter claimed in claim 1, and in particular, that the application reasonably conveys to one of ordinary skill in the art that the Applicants had possession of the elements of claim 1 at the time the Application was filed. Specifically, the Examiner seems to object to claim language "adapting the duration or the amplitude of said programming pulses as a function of the difference between a present state of the one or more

memory cells and a target state of the one or more memory cells." However, as shown below, the claim has ample support in the specification.

With respect to "adapting the duration or the amplitude of said programming pulses", the Examiner is respectfully referred to an embodiment of the invention described at page 24, line 9 to page 25, line 19. In that embodiment, for example, a characteristic of successive programming pulses may increase, either by a fixed or varying increment, allowing for programming of "fast" cells initially and "slow" cells subsequently, using programming pulses of increased duration or amplitude. The Examiner is also referred, for example, to originally filed claims 8 and 32, which recite stepping the programming pulse including by executing steps of unequal time duration.

With respect to "adapting . . . as a function of the difference between a present state of the one or more memory cells and a target state of the one or more memory cells", the Examiner is referred, for example, to page 34, line 10 to page 35, line 15, and in particular, to page 34, lines 11 – 14: "if the threshold voltage level after a programming pulse is measured, it is possible to adjust the voltage level increment of the next programming pulse to move the threshold level toward the program verify level more quickly." The quoted text clearly describes adapting the duration or the amplitude of said programming pulses as a function of the difference between a present state of the one or more memory cells and a target state of the one or more memory cells in such a way to indicate to one of ordinary skill in the relevant art that the Applicants were in possession of the invention at the time the Application was filed. Applicants respectfully request that the Examiner's rejection of claim 1 be withdrawn.

The Examiner also rejected claim 1, stating that the amendment to claim 1 added new matter. Based in part on the reasons and examples stated above, and in view of the remarks that follow, Applicants respectfully traverse the rejection and state that the amendment adds no new matter.

Applicants respectfully traverse this rejection in view of the specification describing the adaptation of the duration or amplitude of the programming pulses applied to either the drain or the gate of one or more memory cells. See, for example, Fig. 9 and the description at page 20, lines 18 – 23:

> When programming with a constant gate voltage VG and a stepped drain voltage VD between 4.5V to 5.5V, the resultant programming times range from of 100μsec down to 0.8μsec, respectively. However, in order to achieve approximately the same programming time range with a constant drain voltage VD, the gate voltage must be stepped from 8V to 11.5V. (Emphasis added)

Accordingly, Applicants respectfully traverse the Examiner's rejection and state that assert that no new matter is added in the amendment. Applicants respectfully request that the Examiner's rejection of claim 1 be withdrawn.

In the Office Action, the Examiner rejected claims 1 – 14 under 35 U.S.C. § 112, second paragraph, for allegedly "omitting essential steps". More specifically, the Examiner asked "what is a voltage condition of the other terminals of the memory cells?" Applicants respectfully traverse the rejection.

With all due respect, the Examiner has confused the breadth of the claim with "omitting essential steps." Various actions may be taken in conjunction with the claimed method elements and remain within the scope of the invention. Those of skill in the art will recognize the voltage conditions required to operate the memory cell may be as appropriate for the desired operation. Applicants respectfully assert that there is no need to limit the claim to particular voltage conditions at other terminals of the memory cells, as these are not essential steps of the claim. Applicants respectfully request that the Examiner withdraw the above stated rejection of claim 1 and its dependent claims, claims 2 – 14.

The Examiner further rejected claim 1 under 35 U.S.C. §112, second paragraph, as being indefinite for allegedly "failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention." More specifically, the Examiner rejected claim 1 because the term "adapting" in claim is a relative term which renders the claim indefinite.

Applicants respectfully traverse this rejection, insofar as the word "adapting" may be broad and encompassing, but it is not indefinite. Applicants assert that one of ordinary skilled in the art would understand the scope of the claim. The Examiner is respectfully directed to numerous locations interspersed throughout the specification wherein the terms "adapting" and "adaptation" have been used. See, for example, the description at page 33:

> Typically, the bit line programming levels increase in voltage by predetermined amounts. Reference is now made to Figs. 15 and 16 which illustrate a further embodiment of the present invention which changes the incremental voltage level of the drain Vppd between pulses in order to program most of the bits in as few programming steps as possible. As described hereinbelow, the incremental voltage level is adapted to the current response of the bit to programming pulse. (emphasis added)

One of ordinary skilled in the art, in view of the prior art and the status of the art, would be reasonably apprised of the scope of the invention. See MPEP §2173.05(b). Accordingly, Applicants respectfully assert that claim 1 is proper under 35 U.S.C. §112, second paragraph and request that the rejection of claim 1 be withdrawn.

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35 U.S.C. § 102 Rejections

The Fong Reference

In the Office Action, the Examiner rejected claims 1-14 under 35 U.S.C. § 102(b), as being anticipated by Fong U.S. Patent No. 5,537,358. The Examiner contended that Fong discloses programming a memory array using programming pulses applied to either the drain or gate of one or more memory cells, comprising adapting the duration or the amplitude of the programming pulses as a function of the difference between a present state of the one or

more memory cells and a target state of the one or more cells, wherein the amplitude or duration of the pulses are correlated to the difference.

Applicants respectfully traverse this rejection in view of the remarks that follow.

In order to make a prima facie rejection by anticipation, the Examiner must show that every element of a claim is present in the prior art. The Examiner has not done so because not every element of claim 1 is disclosed in the prior art. Independent claim 1 recites, inter alia, a method comprising "adapting the duration or the amplitude of said programming pulses as a function of the difference between a present state of the one or more memory cells and a target state of one or more cells, wherein the amplitude or duration of the programming are correlated to the difference between a present state of the one or more memory cells and a target state of the one or more cells." Whereas, Fong teaches:

> A flash memory system including an array of flash memory cells and at least one programmed reference cell and at least one erased reference cell disposed in a common integrated circuit. Memory array read operations are carried out by reading the two reference cells and the target cell of the memory array. The two reference cells produce a programmed reference output and an erased reference output which are averaged to provide a reference value to be compared with the read output of the target cell. In that the reference value is derived by on-chip programmed and erased cells, the reference value will automatically adapt to changes in the fabrication process, temperature, operating voltages and the like. Preferably, the reference cell outputs are also utilized to adaptively control the programming and erasing of the memory array cells so as to control the erased and programmed threshold voltages of the array cells. (Abstract, emphasis added)

That is, the Fong reference discloses comparing a programmed cell to an erased cell. However, nowhere in the above, or anywhere in the Fong reference, for that matter, is there

shown "adapting the duration or the amplitude of said programming pulses as a function of the difference between a present state of the one or more memory cells and a target state of one or more cells."

Furthermore, in col. 12, lines 43 - 52, Fong explicitly states that "the amount of increase in the magnitude of the erase pulse adaptively selected based upon the measured values of Vte and Vtp of the reference cells 10a and 10b located in the same row as the target cells being programmed." Vte and Vtp are the values of the above mentioned voltages of the two reference cells. Fong therefore fails to teach or suggest "adapting the duration or the amplitude of said programming pulses as a function of the difference between a present state of the one or more memory cells and a target state of one or more cells". Rather, the programming pulse voltage levels and duration in Fong are predefined (see Table 3 in Col. 12 and Table 4 in Col. 13), fixed in value and not adapted based on, inter alia, the current state of the cells being programmed.

Applicants, therefore, respectfully request reconsideration and withdrawal of the Examiner's rejection of independent claim 1.

The Khan Reference

In addition, the Examiner stated in the Office action (under the section labeled "Claim Rejections – 35 USC §112") that "it is believed that the rejections of claims 1-14 under 35 U.S.C. 102 by . . . Kahn should be sustained as set forth in the previous Office action." In the previous Office Action, the Examiner rejected claims 1-14 under 35 U.S.C. § 102(b), as being anticipated by Khan U.S. Patent No. 5,870,335. The Examiner claimed that "Kahn's programming method is adapted based on the state of the memory cell after verifying and the program is repeating by incrementally changing a programming current pulse flowing between the source and drain of the selected memory cell until all cells verify as programmed."

Applicants respectfully traverse this rejection in view of the remarks that follow.

Independent claim 1 recites, *inter alia*, "a method for programming a memory array . . . comprising . . . adapting the duration or the amplitude of said programming pulses

as a function of the difference between a present state of the one or more memory cells and a target state of the one or more memory cells, wherein the amplitude or duration of the programming pulses are correlated to the difference between a present state of the one or more memory cells and a target state of the one or more memory cells." Whereas, Khan teaches:

> An integrated circuit memory system and method for precision hot carrier injection programming of single or plurality of nonvolatile memory cells is described. Each program cycle is followed by a verify cycle. Precision programming is achieved by incrementally changing a programming current pulse flowing between the source and drain in the memory cell during successive program cycles and a constant current during successive verify cycles. Current control and voltage mode sensing circuitry reduces circuit complexity, reduces programming cell current, lowers power dissipation, and enables page mode operation. Precision programming is useful for multilevel digital and analog information storage. (Abstract, emphasis added)

Indeed, Khan states that "[m]ultiple program and verify cycles are performed with incrementally changing programming cell current during successive cycles to reduce programming time. The application of programming, verify or read cell voltages and current are performed in a predetermined manner including pre-charging the bitline depending on the characteristics of the particular memory cell type used." (Col. 3, lines 30-36 emphasis added). However, Kahn does not teach nor suggest "adapting the duration or the amplitude of said programming pulses as a function of the difference between a present state of the one or more memory cells and a target state of the one or more memory cells." To the contrary, the programming pulse voltage levels and durations in Khan are predefined, fixed and not adapted based on the state of the cells being programmed. Applicants, therefore, respectfully request reconsideration and withdrawal of the rejections of independent claim 1.

The Cohen Reference

In addition, the Examiner stated (also under the section labeled "Claim Rejections – 35 USC §112") that "it is believed that the rejections of claims 1-14 under 35 U.S.C. 102 by Cohen . . . should be sustained as set forth in the previous Office action." In the previous Office Action, the Examiner rejected claims 1-14 under 35 U.S.C. § 102(a), as being anticipated by Cohen, et al. U.S. Patent No. 6,292,394. In the current Office action, the Examiner claimed that "Cohen's programming method is adapted based on the state of the memory cell such as repeating the program and verify of the selected memory cell until all cells verify as programmed."

Applicants respectfully traverse this rejection in view of the remarks that follow.

Independent claim 1 recites, *inter alia*, "a method for programming a memory array . . . comprising . . . adapting the duration or the amplitude of said programming pulses as a function of the difference between a present state of the one or more memory cells and a target state of the one or more memory cells, wherein the amplitude or duration of the programming pulses are correlated to the difference between a present state of the one or more memory cells and a target state of the one or more memory cells." Whereas the Cohen reference, which is assigned to the assignee of the present application, teaches:

> A method for programming an array having a multiplicity of memory cells. The method includes, per-cell-to-be programmed, verifying a programmed or non-programmed state of the cell and flagging those of the cells that verify as non-programmed during one of the verify steps after having previously verified as programmed. A programming pulse having a programming level is applied to the non-programmed cells which are not flagged cells. The steps of verifying, flagging and applying are then repeated until all of the cells verify as programmed at least once. Subsequently, a boost pulse having a boost

programming level lower than the programming level is applied to the flagged cells. (Abstract)

Cohen further teaches coarse and fine programming steps, and indeed discloses stepping a programming pulse. However, Cohen does not teach "adapting the duration or the amplitude of said programming pulses as a function of the difference between a present state of the one or more memory cells and a target state of the one or more memory cells" as disclosed in claim 1 of the present application.

In view of the above remarks, because claims 2 through 14 depend directly or indirectly from claim 1, Applicants respectfully assert claims 2-14 to be allowable by virtue of their dependence on an allowable base claim.

In view of the foregoing amendments and remarks, the pending claims are deemed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 05-0649.

Respectfully submitted,

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Dated: December 17, 2003

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